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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,028	04/27/2006	Kyoung-Ju Shin	AB-1883 US	9578

32605 7590 10/02/2008

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2871	

MAIL DATE	DELIVERY MODE
10/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,028	SHIN ET AL.	
	Examiner	Art Unit	
	THANH-NHAN P. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-12* is/are rejected.

7)☒ Claim(s) *6,7,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al (US 2002/0145684) in view of Den Boer et al (US 6,243,062).

Watanabe et al disclose (Figs. 4a - 4c) a thin film diode array panel comprising:

Claims 1 and 2:

- an insulating substrate (20)
- first floating electrode (62) made of an opaque conductor, formed on the insulating substrate
- an insulating layer (63) formed on the first floating electrode
- a first gate line (51) including a first input electrode (64a) overlapping the first floating electrode (32) where the insulating layer is interposed between the first input electrode and the first floating electrode
- a pixel electrode (66) including a first contact electrode (64b) overlapping the first floating electrode where the insulating layer is interposed between the first contact electrode and the first floating electrode

- wherein the pixel electrode and the first gate line are made of indium tin oxide (par. 0059)

Watanabe et al lack disclosure of:

- a first and second redundant gate lines made of an opaque conductor and formed on the insulating substrate; wherein the first and second redundant gate lines made of Mo
- a second floating electrode made of an opaque conductor
- a first gate line formed on the first redundant gate line, and a second gate line formed on the second redundant gate line and including a second input electrode overlapping the second floating electrode where the insulating layer is interposed between the second input electrode and the second floating electrode
- second contact electrode overlapping the second floating electrode where the insulating layer is interposed between the second contact electrode and the second floating electrode, and a main body

In summary, the main difference between the reference by Watanabe et al and the present invention is that Watanabe et al disclose a single MIM diode instead of a dual MIM diode, and Watanabe et al disclose one-layered gate line instead of double-layered gate line.

However, it is well known in the art to form double-layered (or multi-layered) gate line, for the benefit of preventing the corrosion.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form redundant gate lines, wherein the redundant gate lines made of Mo, for the benefit of preventing the corrosion.

Further, it is also well known in the art to use a dual MIM diode for the benefit of improving response time and reducing the potential for crosstalk or image retention, as evidenced by Den Boer et al, (Fig. 6; Abstract; col. 12, lines 11-66; col. 13, lines 1-67).

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a dual MIM diode for the benefit of improving response time and reducing the potential for crosstalk or image retention.

Claim 3:

- wherein the insulating layer (63) includes a first insulating layer regionally formed around the first floating electrode (62)

From the argument above in claim 1, it would have been obvious to have a second insulating layer regionally formed around the second floating electrode; thus, it does not patentably distinguish the invention.

Claims 4 and 5:

Similarly, it would have been obvious to have the insulating layer covers the first and second redundant gate lines and the first and second floating electrodes and has contact holes exposing the first and second redundant gate lines.

Further, even though Watanabe et al lack disclosure of the first and second gate lines are connected to the first and second redundant gate lines through the contact holes; the insulating layer covers the first and second redundant gate lines and the first

and second floating electrodes and has cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the cutout stripes, it would have been obvious to one of ordinary skill in the art to have the gate lines and the redundant gate lines connected through the contact hole or through the cutout stripes of the insulating layer, at least for the benefit of obtaining more secure/contact between the two layers/two lines.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the gate lines and the redundant gate lines connected through the contact hole or through the cutout stripes of the insulating layer, at least for the benefit of obtaining more secure/contact between the two layers/two lines.

Claims 8-12 are met the discussion regarding claims 1-5 rejection above, respectively.

Allowable Subject Matter

Claims 6, 7, 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reason for allowance: There is no prior art of record that teaches or suggests a thin film diode array panel comprising a relationship of various elements as claimed with the specific allowable subject matter cited in the following claims:

Claims 6 and 13:

- wherein the insulating layer has a cutout disposed to overlap at least a portion of the main body of the pixel electrode

Claim 7 is allowed since it depends on allowed claim 6.

Claim 14 is allowed since it depends on allowed claim 13.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,909,264.

US 5,893,621.

US 5,107,355.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

-- *September 30, 2008*
TN

/David Nelms/

Supervisory Patent Examiner, Art Unit 2871